REMARKS/ARGUMENTS

Claims 1, 3-13, and 15-25 are pending in this application, stand finally rejected, and are at issue herein. While the Office Action indicates that claims 2 and 14 are pending and rejected, the applicant respectfully submits that these claims were canceled in response to the previous Office Action. Reconsideration of claims 1, 3-13, and 15-25 in view of the following remarks and indication of their allowability at an early date are respectfully solicited.

The applicant wishes to thank the Examiner for consideration of the corrected drawings received on November 15, 2004, and the indication of acceptability thereof.

The applicant also wishes to thank the Examiner for consideration of the specification received on November 15, 2004, and the indication of acceptance thereof as well.

The Examiner has rejected claims 1, 3-11, 13, and 15-25 (mistakenly identified as 1-11 and 13-25) under 35 U.S.C. §102(e) as being anticipated by Pecore (U.S. Patent No. 6,014,325). The applicant has again thoroughly considered the teachings of Pecore '325 and the Examiner's rational for continued assertion thereof, but must respectfully maintain the traversal of this ground of rejection. Reconsideration of this ground of rejection and indication of the allowability of claims 1, 3-11, 13, and 15-25 in view of the following remarks are respectfully solicited.

As previously argued by the applicant, independent claim 1 and those claims dependent thereon require, *inter alia*, that the second DC output stage have a regulated DC output inverted by an inverter connected to the second wave rectifier to be the first polarity. In this way, the dual output transformerless power supply provides either dual positive or dual negative outputs.

As discussed by the applicant in the previous response, and as asserted by the Examiner, Fig. 2 of Pecore '325 shows two regulated DC outputs of the same polarity. However, neither this circuit nor any teaching of Pecore '325 includes or describes the use of an inverter connected to the second wave rectifier as required by this independent claim 1. The Examiner has not contradicted this point, but instead relies upon an unrelated definition of the term "inverter" from the IEEE Dictionary to state that the applicant's invention does not include an inverter. However, the Examiner has selected a definition of the term inverter that has nothing to do with the usage of that term in the present application, and is clearly not

the only way that this term is used in the art. Indeed, the Federal Circuit has repeatedly cautioned against the indiscriminate use of dictionary definitions. Indeed, when a term has several definitions, the Examiner must look to the intrinsic record of the specification and claims to see how a particular term is used therein.

In this case, the applicants have used the term inverter in accordance with its common usage in the art to identify a class of circuit elements that invert the polarity of a signal from its input to its output. For example, as described in paragraph [0010], this class of circuit elements may include a transistor in either the common emitter configuration or the common source configuration. Such a configured transistor is commonly known in the art as an inverter because it inverts the polarity of the signal applied to it without modifying the magnitude thereof. When this term is interpreted in view of the specification and in view of its common usage in the art, it is clear that the applicant's claimed invention does indeed include an inverter. This notwithstanding an alternate definition of the term "inverter" as used in the electric power context as a machine, device, or system that changes direct current power to alternating current power. Indeed, there is no support in the specification that would allow for such an interpretation of the term "inverter" as the specification is clear that the dual output of the transformerless power supply is either dual positive or dual negative DC power. As such, the Examiner's contention that "the applicant's transistor is not an inverter" is erroneous and should not be maintained. When the correct interpretation of the term "inverter" is applied, it is clear that Pecore '325 does not anticipate this claim.

The Examiner has also argued that even if the transistor disclosed by the applicant is an inverter, the transistor of Pecore '325 illustrated in Fig. 2 as reference number 142 is also an inverter. However, as pointed out in the applicant's previous response, this transistor does not invert the polarity of a signal connected to its input, but instead operates as a power switch to shut off the output voltage. Specifically, column 7, line 51 of Pecore '325 describes that the transistor is part of "a switching circuit 107 ... to short together terminals 116 and 113 of the 24 VDC stage in response to a control signal CS applied at terminal 115. By shorting these load terminals together, capacitor 132 cannot build up a potential sufficient to cause current to flow through zener diodes 134 and 136 ... . This reduces the voltage across terminals 116 and 113 to a magnitude equal to the collector-emitter saturation voltage of voltage of transistor 142, or about 0.1 volts." This 0.1 volts is the same polarity as the output voltage across these terminals when the transistor is not turned on (24 VDC). As such, this transistor 142 does not provide any inverting operation, and therefore cannot anticipate an inverter. Transistor 142 of Pecore '325 is used as a power switch in the switching circuit "to reduce power consumption to near zero." Pecore '325, column 8, lines 15-16, 19-20.

Nowhere in Pecore '325 is this transistor described as providing any inversion of the polarity of a signal.

In view of the above, the applicant respectfully submits that claims 1, and 2-11 dependent thereon are not anticipated by Pecore '325 for the reasons stated above.

Further, independent claim 13 requires a means for inverting the second DC output signal to be the first polarity. As discussed above, Pecore '325 does not include any means for inverting the second DC output signal to be the first polarity. Therefore, Pecore '325 also cannot anticipate claims 13 and 16-21 dependent thereon.

Similarly, independent claim 22 includes means for inverting that is connected to the second means for voltage regulation in that claim. Therefore, Pecore '325 cannot anticipate this claim.

Independent claim 23 includes the step of converting the AC input during a second half cycle to a second DC output with the same polarity as the first DC output by inverting the second DC output. Since Pecore '325 does not include any such inverting of the DC output, it cannot anticipate this claim 23 or claims 24-25 dependent thereon.

With regard to claim 15, the Examiner has also looked to an unrelated dictionary definition of the term "phase shift" to state that the applicant's invention does not provide for phase shifting as defined by the Examiner in this Office Action. However, independent claim 15 requires "means for shifting said AC input 180 degrees for input into second means for rectifying." As is made clear by the applicant, and as is commonly used in the art, the phase shifting by 180 degrees effectively inverts the polarity of the AC signal. As described by the applicant in paragraph [0029], "during the negative-half cycle of the AC input signal, a transistor in either a common emitter or common source configuration may be used to shift the AC input signal by 180 degrees. This shifted voltage is then applied to a second rectifier for converting the shifted AC input voltage into a pulsating DC output signal. ... The second power supply will have the same polarity as the first power supply." As is recognized by those skilled in the art and as is described in the originally filed specification, the applicant's invention as claimed in claim 15 does indeed include phase shifting of the AC input voltage signal by 180 degrees. Since the system of Pecore '325 does not include any such phase shifting by 180 degrees, it cannot anticipate this independent claim 15. Reconsideration of this ground of rejection in view of the actual usage of this phrase in the originally filed specification and the lack of any similar teaching in Pecore '325 is respectfully solicited.

The Examiner has also maintained the rejection of claim 12 under 35 U.S.C. §103(a) as being obvious over Pecore '325 and Tanoi (U.S. Patent No. 5,498,991). The applicant has again thoroughly studied each of these references, the Examiner's rational for combining same, the Examiner's response to the applicant's previous argument, and the language of claim 12. In view of this analysis, the applicant must respectfully maintain the traversal of this ground of rejection. Reconsideration of this ground of rejection and indication of the allowability of claim 12 at an early date are respectfully solicited.

As discussed at length above, Pecore '325 does not include an inverter as required by independent claim 1 from which this claim depends. Since a *prima facie* case of obviousness can only be established if each and every limitation of the claims are taught or suggested by the references as combined, since Pecore '325 does not provide any teaching or suggestion of an inverter, and since Tanoi '991 fails to overcome this deficiency, the applicant respectfully submits that a *prima facie* case of obviousness has not been established with regard to claim 12. Reconsideration of this ground of rejection and indication of the allowability thereof at an early date are therefore respectfully solicited.

The applicant also argued that there is no suggestion or motivation to support this proposed combination of references because the system of Pecore '325 does not have any extremely high voltage signals or extremely low voltage signals from which the microprocessor must be protected. As discussed in the previous response, the system of Pecore '325 is a closed system for use in a refrigeration appliance which utilizes a standard input line voltage to generate an output 24 volt DC signal and an output 5 volt DC signal. As such, there is no reasons to believe that the controller would ever be subjected to extremely high voltage signals as suggested by the Examiner. The Examiner has stated that applying a voltage of 24 volts to a microprocessor that is typically powered by 1.8 VDC – 3.3 VDC may damage the microprocessor. Such speculation finds no support in the references cited by the Examiner. It is not appropriate for the Examiner to create artificial problems not described or reasonably suggested by a reference simply to support the combination of that reference with another for the sole purpose of rejecting the claims of the present application. As such, the applicant maintains that there is no proper suggestion or motivation that could support the combination of the references as proposed by the Examiner.

In view of the above, the applicant respectfully submits that claim 12 is not rendered obvious by the combination of references set forth by the Examiner. Reconsideration of claim 12 and indication of its allowability at an early date are respectfully solicited.

In view of the Examiner's continued assertion of these grounds of rejection based on the application of unrelated definitions from an external dictionary without regard for the usage of these terms as described in the originally filed specification and claims, the applicant has also filed herewith a Notice of Appeal to the Board of Patent Appeals and Interferences.

In view of the above, the applicant respectfully submits that claims 1, 3-13, and 15-25 are in condition for allowance. Reconsideration of claims 1, 3-13, and 15-25 at an early date and indication of their allowability are therefore respectfully solicited.

If the Examiner believes that a telephonic conversation will aid in the resolution of any issues not resolved herein, the Examiner is invited to contact the applicant's attorney at the telephone number listed below.

Respectfully submitted,

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